

# BUV21

## SWITCHMODE™ Series NPN Silicon Power Transistor

This device is designed for high speed, high current, high power applications.

### Features

- High DC Current Gain:  
 $h_{FE} \text{ min} = 20$  at  $I_C = 12 \text{ A}$
- Low  $V_{CE(sat)}$ ,  $V_{CE(sat)}$   
 $\text{max} = 0.6 \text{ V}$  at  $I_C = 8 \text{ A}$
- Very Fast Switching Times:  
 $TF \text{ max} = 0.4 \mu\text{s}$  at  $I_C = 25 \text{ A}$
- Pb-Free Package is Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(SUS)}$	200	Vdc
Collector-Base Voltage	$V_{CBO}$	250	Vdc
Emitter-Base Voltage	$V_{EBO}$	7	Vdc
Collector-Emitter Voltage ( $V_{BE} = -1.5 \text{ V}$ )	$V_{CEX}$	250	Vdc
Collector-Emitter Voltage ( $R_{BE} = 100 \Omega$ )	$V_{CER}$	240	Vdc
Collector-Current – Continuous	$I_C$	40	Adc
– Peak ( $PW \leq 10 \text{ ms}$ )	$I_{CM}$	50	Apk
Base-Current Continuous	$I_B$	8	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	250	W
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to 200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$\theta_{JC}$	0.7	$^\circ\text{C/W}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

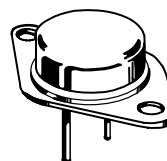
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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**40 AMPERES  
NPN SILICON POWER  
METAL TRANSISTOR  
200 VOLTS – 250 WATTS**



TO-204AE (TO-3)  
CASE 197A

### MARKING DIAGRAM



BUV21 = Device Code  
G = Pb-Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week  
MEX = Country of Origin

### ORDERING INFORMATION

Device	Package	Shipping
BUV21	TO-204	100 Units / Tray
BUV21G	TO-204 (Pb-Free)	100 Units / Tray

# BUV21

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b> (Note 1)				
Collector–Emitter Sustaining Voltage ( $I_C = 200\text{ mA}$ , $I_B = 0$ , $L = 25\text{ mH}$ )	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: ( $V_{CE} = 250\text{ V}$ , $V_{BE} = -1.5\text{ V}$ )( $T_C = 25^\circ\text{C}$ unless otherwise noted) ( $V_{CE} = 250\text{ V}$ , $V_{BE} = -1.5\text{ V}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$		3.0 12.0	mAdc
Collector–Emitter Cutoff Current ( $V_{CE} = 160\text{ V}$ )	$I_{CEO}$		3.0	mAdc
Emitter–Base Reverse Voltage ( $I_E = 50\text{ mA}$ )	$V_{EBO}$	7		V
Emitter–Cutoff Current ( $V_{EB} = 5\text{ V}$ )	$I_{EBO}$		1.0	mAdc
<b>SECOND BREAKDOWN</b>				
Second Breakdown Collector Current with base forward biased ( $V_{CE} = 20\text{ V}$ , $t = 1\text{ s}$ ) ( $V_{CE} = 140\text{ V}$ , $t = 1\text{ s}$ )	$I_{S/b}$	12 0.15		Adc

## ON CHARACTERISTICS

 (Note 1)

DC Current Gain ( $I_C = 12\text{ A}$ , $V_{CE} = 2\text{ V}$ ) ( $I_C = 25\text{ A}$ , $V_{CE} = 4\text{ V}$ )	$h_{FE}$	20 10	60	
Collector–Emitter Saturation Voltage ( $I_C = 12\text{ A}$ , $I_B = 1.2\text{ A}$ ) ( $I_C = 25\text{ A}$ , $I_B = 3\text{ A}$ )	$V_{CE(sat)}$		0.6 1.5	Vdc
Base–Emitter Saturation Voltage ( $I_C = 25\text{ A}$ , $I_B = 3\text{ A}$ )	$V_{BE(sat)}$		1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ( $V_{CE} = 15\text{ V}$ , $I_C = 2\text{ A}$ , $f = 4\text{ MHz}$ )	$f_T$	8.0		MHz
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## SWITCHING CHARACTERISTICS

 (Resistive Load)

Turn-on Time	( $I_C = 25\text{ A}$ , $I_{B1} = I_{B2} = 3\text{ A}$ , $V_{CC} = 100\text{ V}$ , $R_C = 4\ \Omega$ )	$t_{on}$	1.0	$\mu\text{s}$
Storage Time		$t_s$	1.8	
Fall Time		$t_f$	0.4	

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

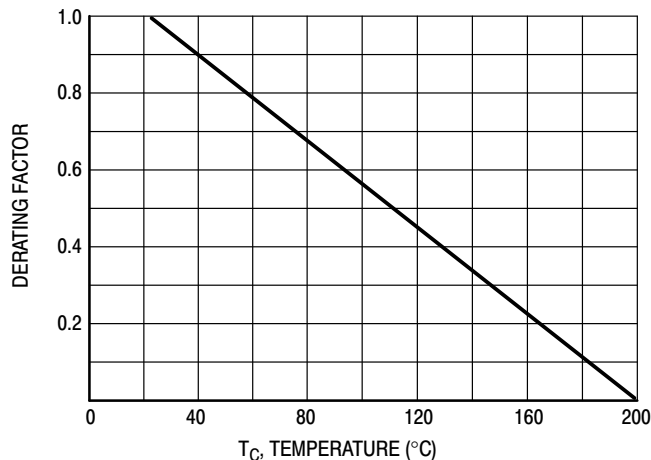


Figure 1. Power Derating

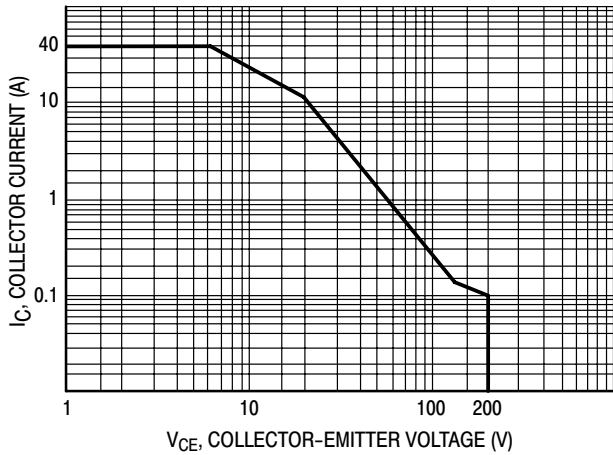


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_C = 25^\circ C$ ,  $T_{J(pk)}$  is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

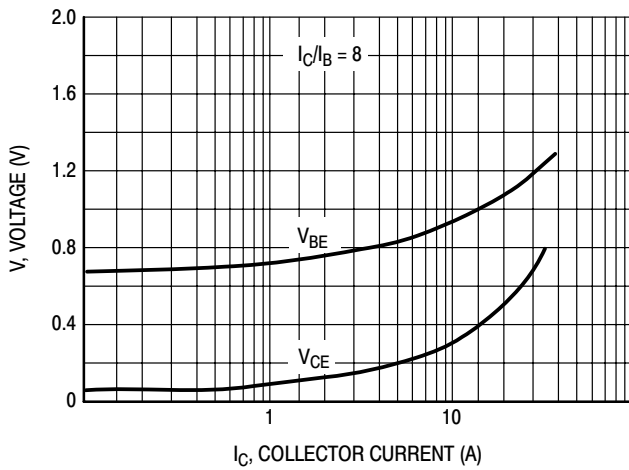


Figure 3. "On" Voltages

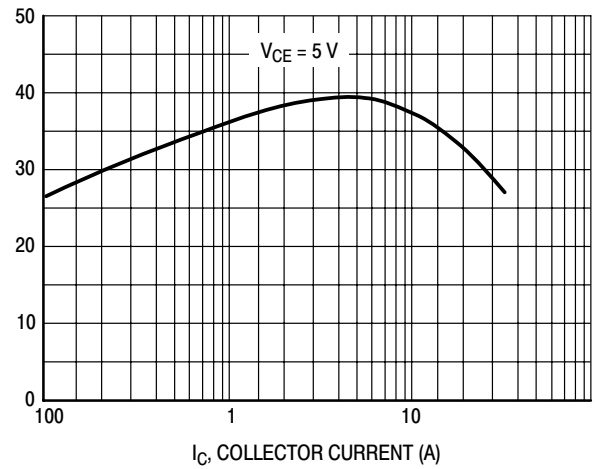


Figure 4. DC Current Gain

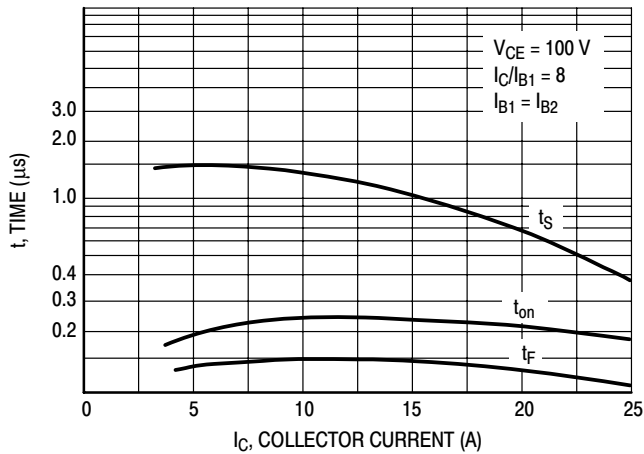
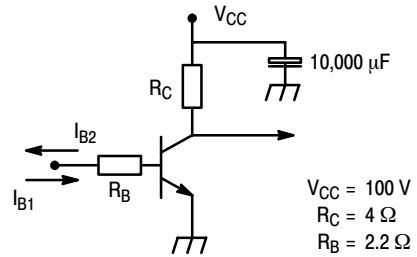


Figure 5. Resistive Switching Performance



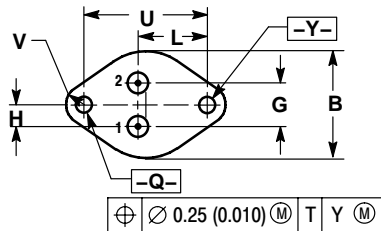
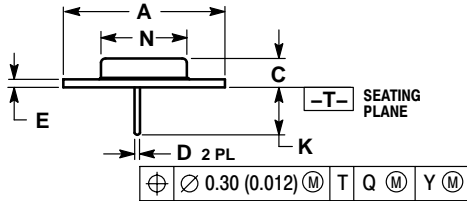
$R_C - R_B$ : Non inductive resistances

Figure 6. Switching Times Test Circuit

# BUV21

## PACKAGE DIMENSIONS


### TO-204 (TO-3) CASE 197A-05 ISSUE K



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

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